Myung SSD
SATA-III F300 Series (6Gbps)

Product Specification

Jan / 2012
Rev. 0.1

MYUNG INFO.TECH.
Myung Information Technologies Co., Ltd.

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1. Revision History

- Rev. 0.1 (2011.11.14) : Preliminary Specification

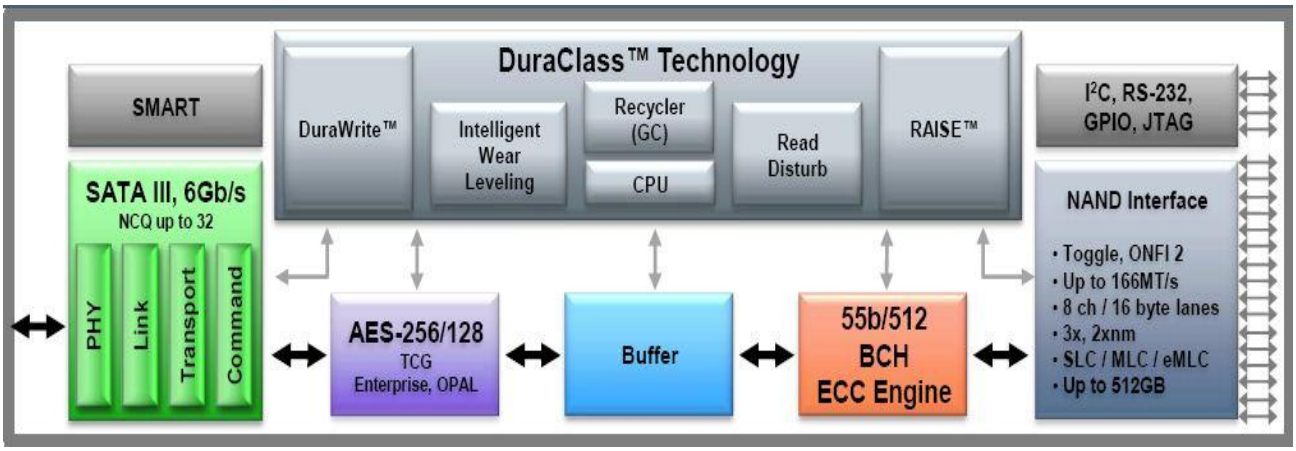
2. General Description

Since Myung's SSD is composed of semiconductor chips, it is resistive on a external shock and does not produce any heat or noise. Since it does not have any moving parts, it is designed to minimize total electricity consumption. It is strongly resistive on dusts and other small particles. We are adopting latest technology of wear-leveling and which increased endurance of our product. Embedded error correction code(ECC) function of the products also guaranty integrity of data stored on the SSD. Myung's SSD has an exceeding reading and writing speed and it is fully compatible with other storage devices in a gaming systems, laptops and PCs.

3. Features

- Fully SATA 6.0Gbps compatible
- Uses 2Xnm NAND flash memory Multi Level Cell (MLC) components.
- Uses SandForce® SF-2281
- Native Command Queuing(NCQ) up to32 commands
- ECC(Error Correction Code)
  - Max 55 bits/512B Sector (BCH)
  - Uncorrectable bit Error Rate 10^{-16}
- Flash Management Features
  - Bad block management
  - Dynamic and static wear-leveling
- Power Management Features
- SMART Features
  - Self-Monitoring,
  - Analysis and Reporting Technology
- Security Features
- TRIM (requires OS support)
- Storage Capacity
  - 64GB / 128GB / 256GB / 512GB
- Temperature
  - Operating Temp : 0°C ~ 70°C
  - Non – operating Temp : - 45°C ~ 85°C
- Ordering Information
  - MITSF300-064G : SATA III MLC 64GB
  - MITSF300-128G : SATA III MLC 128GB
  - MITSF300-256G : SATA III MLC 256GB
  - MITSF300-512G : SATA III MLC 512GB

4. Block Diagram



5. Specifications

Mechanical Specifications		
Form Factor		3.5 Inch
Dimensions (mm)	**Length**	146 mm
	Width	101.4 mm
	Height	14 mm
Connector	SATA 7+15 pins combo connector	

Electrical Specifications					
Parameter	**Symbol**	MIN	TYP	MAX	UNIT
Voltage Input	**VCC**	4.0	5.0	5.25	V

Weight of Capacities				
Capacity	64GB	128 GB	256 GB	512 GB
Weight	230 g	230 g	230 g	230 g

Performance of Capacities				
Capacities	64GB	128GB	256GB	512GB
Max Read 6Gbps1	up to 550 MB/s	up to 550 MB/s	up to 550 MB/s	up to 550 MB/s
Max Write 6Gbps[1]	up to 500 MB/s	up to 500 MB/s	up to 520 MB/s	up to 520 MB/s
Max Read 3Gbps1	up to 280 MB/s	up to 280 MB/s	up to 280 MB/s	up to 280 MB/s
Max Write 3Gbps[1]	up to 260 MB/s	up to 260 MB/s	up to 260 MB/s	up to 260 MB/s
4KB Random Read[2]	20,000 IOPS (75 MB/s)	20,000 IOPS (75 MB/s)	40,000 IOPS (155 MB/s)	50,000 IOPS (195 MB/s)
4KB Random Write[2]	60,000 IOPS (235 MB/s)	60,000 IOPS (235 MB/s)	60,000 IOPS (235 MB/s)	40,000 IOPS (155 MB/s)
Max 4KB Random Write[3]	85,000 IOPS (330 MB/s)	85,000 IOPS (330 MB/s)	85,000 IOPS (330 MB/s)	40,000 IOPS (155 MB/s)
Sequential Read AS-SSD	425 MB/s	500 MB/s	510 MB/s	495 MB/s

System Configuration: Intel® Core™ i5 2500K processor, ASUS P8P67 Deluxe Board, Microsoft Windows 7 Ultimate

User Addressable Sectors	
Unformatted Capacity	**Total User Addressable Sectors in LBA Mode**
60GB	117,231,408
120GB	234,441,648
240GB	468,862,128
480GB	937,703,088

Power Consumption		
Capacity	**Idle (typical)**	**Active (typical)**
64GB	0.43W	2.65W
128GB	0.43W	2.65W
256GB	0.43W	2.65W
512GB	0.43W	2.65W

- Note : I/O performance is measured using Iometer2008, Queue Depth 32

6. Reliability Characteristics

Temperature	
Operating	0°C ~ 70°C
Non-operation	- 45°C ~ 85 °C
Humidity	
Operating	60°C, 93%R.H
Altitude	
Non-Operating	80,000 feet
Random Vibration note 1	
Non-Operating	15Hz ~ 2,000Hz
Shock	
Non-Operating	1,500g / 0.5ms

- Note 1: Random Vibration Grms 16.32 / TEST X, Y, Z
  Shock TEST ±X, ±Y, ±Z

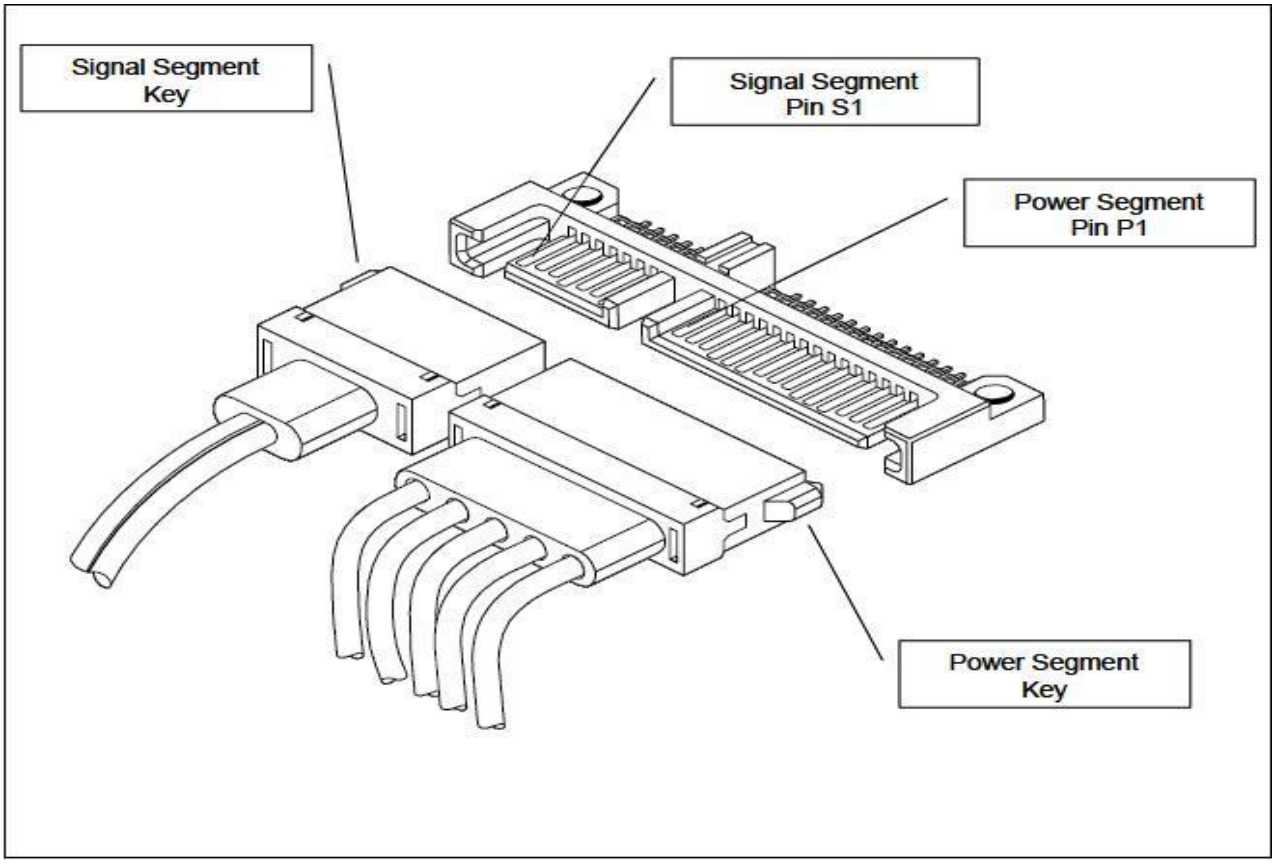
Wear-Leveling algorithm
Myung's SSD supports static/dynamic wear leveling. When the host writes data, the Controller will find and use the block with the lowest erase count among the free blocks. This is known as dynamic wear leveling. When the free blocks' erase count is higher than the data blocks', it will activate the static wear leveling, replacing the not so frequently used user blocks with the high erase count free blocks.

ECC algorithm
The controller use BCH code option
BCH: Max 55 bits/512B sector

Bad-block management
When the flash encounters ECC failed, program fail or erase fail, the controller will mark the block as bad block to prevent the used of this block and caused data lost later on.

7. SATA Connector Descriptions

7-1 Connector locations



7-2 SATA Pinout Data

Segment	Pin No.	Signal Name	Signal Description
Signal segment	S1	GND	2nd mate
	S2	A+	Differential signal pair A From phy
	S3	A-	
	S4	GND	2nd mate
	S5	B-	Differential signal pair B From phy
	S6	B+	
	S7	GND	2nd mate

7-3 SATA Pinout Power

Power segment	P1	V33	3.3V POWER (Not used)
	P2	V33	3.3V POWER (Not used)
	P3	V33	3.3V power, pre-charge, 2nd mate
	P4	GND	1st mate
	P5	GND	2nd mate
	P6	GND	2nd mate
	P7	V5	5V power, pre-charge, 2nd mate
	P8	V5	5V POWER
	P9	V5	5V POWER
	P10	GND	2nd mate
	P11	Reserved	-
	P12	GND	1st mate
	P13	V12	12V power, pre-charged, 2nd mate
	P14	V12	12V (Not used)
	P15	V12	12V (Not used)

▶ Note
- All pins are in a single row, with a 1.27 mm (.050”) pitch.
- There are total of 7pins in the signal segment and 15pins in the power segment.

8. Supports ATA Command

COMMAND NAME	COMMAND CODE (HEX)
CHECK POWER MODE	E5h
DATA SET MANAGEMENT	06h
DEVICE CONFIGURATION OVERLAY **	B1h
DOWNLOAD MICROCODE	92h
DOWNLOAD MICROCODE DMA	93h
EXECUTE DEVICE DIAGNOSTIC	90h
FLUSH CACHE	E7h
FLUSH CACHE EXT	EAh
IDENTIFY DEVICE	ECh
IDLE	E3h
IDLE IMMEDIATE	E1h
INITIALIZE DEVICE PARAMETERS	91h
NOP	00h
READ BUFFER	E4h
READ BUFFER DMA	E9h
READ DMA EXT	25h
READ DMA WITHOUT RETRIES	C9h
READ FPDMA QUEUED	60h
READ LOG DMA EXT	47h
READ LOG EXT	2Fh
READ LONG	22h
READ LONG WITHOUT RETIY	23h
READ MULTIPLE	C4h
READ MULTIPLE EXT	29h
READ NATIVE MAX ADDRESS	F8h
READ NATIVE MAX ADDRESS EXT **	27h
READ SECTOR(S) EXT	24h
READ SECTORS WITHOUT RETRY	21h
READ VERIFY SECTOR(S)	40h
READ VERIFY SECTOR(S) (without Retry)	41h
READ VERIFY SECTOR(S) EXT	42h
RECALIBRATE	10h
REQUEST SENSE DATA EXT	0Bh
SANITIZE DEVICE **	B4h
SECURITY DISABLE PASSWORD	F6h
SECURITY ERASE PREPARE	F3h
SECURITY ERACE UNIT	F4h
SECURITY FREEZE LOCK	F5h
SECURITY SET PASSWORD	F1h
SECURITY UNLOCK	F2h

COMMAND NAME	COMMAND CODE (HEX)
SEEK	70h
SET FEATURES	EFh
SET MAX ADDRESS	F9h
SET MAX ADDRESS EXT **	37h
SET MULTIPLE MODE	C6h
SLEEP	E6h
SMART	B0h
STANDBY	E2h
STANDBY IMMEDIATE	E0h
TRUSTED NON-DATA *	5Bh
TRUSTED RECEIVE *	5Ch
TRUSTED RECEIVE DMA *	5Dh
TRUSTED SEND *	5Eh
TRUSTED SEND DMA *	5Fh
WRITE BUFFER	E8h
WRITE BUFFER DMA	EBh
WRITE DMA EXT	35h
WRITE DMA WITHOUY RETRIES	CBh
WRITE FPDMA QUEUED	61h
WRITE LOG DMA EXT	57h
WRITE LOG EXT	3Fh
WRITE LONG	32h
WRITE LONG (without Retry)	33h
WRITE LONG WITHOUT RETRY	33h
WRITE MULTIPLE	C5h
WRITE MULTIPLE EXT	39h
WRITE SECTOR(S) EXT	34h
WRITE SECTORS WITHOUT RETRY	31h
WRITE UNCORRECTABLE EXT	45h

* Only supported in TCG Security enabled FW
** Will be implemented post MP1

9. SMART

9-1 SMART subcommand sets

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Function Set command. The subcommands are

Command	Command Code
SMART read attributes	D0
SMART read threshold	D1*
SMART enable/disable attributes auto save	D2
SMART save attributes values	D3*
SMART execute off-line immediate	D4
SMART read log sector	D5
SMART write log sector	D6
SMART write attribute threshold	D7*
SMART enable operations	D8
SMART disable operations	D9
SMART return status	DA

* Note that D1, D3 and D7 are supported, but have been made obsolete in the ATA-8ACS-2 specification.

9-2 SMART Attributes

The SMART Attribute Sector defines attribute format. The following SMART Attribute data structure is implemented for the device.

9-2-1 SMART Attribute Data Structure

Byte	Description
0 : 1	SMART structure version number
2 : 361	1st - 30th Individual attribute data (Vendor Specific)
362	Off-line data collection status
363	Self-test execution status
364 : 365	Total time in seconds to complete off-line data collection activity
366	Reserved
367	Off-line data collection capability
368 : 369	SMART capability

370	Error logging capability (bit 0 set=device error logging supported)
371	Self-test failure check point (Vendor Specific
372	Short self-test routine recommended polling time(in minutes)
373	Extended self-test routine recommended polling time(in minutes)
374 ~ 510	Reserved
511	Data structure checksum

9-2-2 Attribute ID Numbers

ID	Attribute Name	ID	Attribute Name
1	Raw Read Error Rate *	200	Total Count of Read Commands
9	Power-On Hours	201	Total Count of Write Commands
12	Power Cycle Count	202	Total Count of Error Bits from Flash
184	Initial Bad Block Count	203	Total Count of Read Sectors with Correctable Bit Errors
195	Program Failure Block Count	204	Bad Block Full Flag
196	Erase Failure Block Count	205	Maximum PE Count Specification
197	Read Failure Block Count (Uncorrectable Bit Errors)	206	Minimum Erase Count
198	Total Count of Read Sectors	207	Maximum Erase Count
199	Total Count of Write Sectors	208	Average Erase Count

* indicates that the corresponding Attribute Values is fixed value for compatibility.

9-3 SMART Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature.

9-4 SMART Execute Off-line Immediately (subcommand D4h)

This subcommand causes the device to start the off-line process for the requested mode and operation. The LBA Low register shall be set to specify the operation to be executed.

LBA Low	Description
00h	Execute SMART off-line data collection routine immediately
01h	Execute SMART Short self-test routine immediately in off-line mode
02h	Execute SMART Extended self-test routine immediately in off-line mode
04h	Execute SMART Selective self-test routine immediately in off-line mode
81h	Execute SMART short self-test routine immediately in captive mode
82h	Execute SMART Extended self-test routine immediately in captive mode
84h	Execute SMART selective self-test routine immediately in captive mode

9-5 SMART Read Log Sector (subcommand D5h)

This command returns the specified log sector content to the host. LBA Low and Sector Count registers shall be set to specify the log sector and sector number to be written.

Log Sector Address	Smart Log	Content	
00h	N	Log directory	Read Only
07h	N	Extended SMART Self-Log	Read Only
09h	Y	Selective Self-Test Log	Read – Write
10h	N	NCQ Command Error Log	Read – Write
11h	Y	SATA Log	Read Only
B7h	Y	SSD Event Log	Read Only
E0h	Y	SCT Host Command Status Log	Read – Write
E1h	Y	SCT Host Data Log	Read – Write
FBh	N	System Event Log	Read Only

9-5-1 SMART Log Directory

Byte	Description
0~1	SMART Logging Version (set to 01h)
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved
...	
510	Number of sectors in the log at log address 255
511	Reserved

9-5-2 SMART summary error log sector

Byte	Description
0	SMART error log version (set to 01h)
1	Error log index
2~91	First error log data structure
92~181	Second error log data structure
182~271	Third error log data structure
272~361	Fourth error log data structure
362~451	Fifth error log data structure
452~453	Device error count
454~510	Reserved
511	Data Structure checksum

Error log data structure

Byte	Description
n ~ n+11	First command data structure
n+12 ~ n+23	Second command data structure
n+24 ~ n+35	Third command data structure
n+36 ~ n+47	Fourth command data structure
n+48 ~ n+59	Fifth command data structure
n+60 ~ n+89	Error data structure

Command data structure

Byte	Description
n	Content of the Device Control register when the Command register was written
n+1	Content of the Features Control register when the Command register was written
n+2	Content of the Sector Count Control register when the Command register was written
n+3	Content of the LBA Low register when the Command register was written
n+4	Content of the LBA Mid register when the Command register was written
n+5	Content of the LBA High register when the Command register was written
n+6	Content of the Device/Head register when the Command register was written
n+7	Content written to the Command register
n+8	Timestamp
n+9	Timestamp
n+10	Timestamp
n+11	Timestamp

Error data structure

Byte	Description
n	Reserved
n+1	Content written to the Error register after command completion occurred.
n+2	Content written to the Sector Count register after command completion occurred
n+3	Content written to the LBA Low register after command completion occurred
n+4	Content written to the LBA Mid register after command completion occurred.
n+5	Content written to the LBA High register after command completion occurred.
n+6	Content written to the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 – n+26	Extended error information
n+27	State
n+28	Life Timestamp (least significant byte)
n+29	Life Timestamp (most significant byte)

State field values

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
3h	x Active/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xAh	Reserved
xBh-xFh	Vendor unique

9-5-3 Self-test log structure

Byte	Description
0~1	Data structure revision
n*24+2	Self-test number
n*24+3	Self-test execution status
n*24+4~n*24+5	Life timestamp
n*24+6	Self-test failure check point
n*24+7~n*24+10	LBA of first failure
n*24+11~n*24+25	Vendor specific
.....	.....
506~507	Vendor specific
508	Self-test log pointer
509~510	Reserved
511	Data structure checksum

N is 0 through 20.
The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

9-5-4 Selective self-test log structure

Byte	Content	
0-1	Data structure revision	Read and Write
2-9	Starting LBA for test span 1	Read and Write
10-17	Ending LBA for test span 1	Read and Write
18-25	Starting LBA for test span 2	Read and Write
26-33	Ending LBA for test span 2	Read and Write
34-41	Starting LBA for test span 3	Read and Write
42-49	Ending LBA for test span 3	Read and Write
50-57	Starting LBA for test span 4	Read and Write
58-65	Ending LBA for test span 4+	Read and Write
66-73	Starting LBA for test span 5	Read and Write
74-81	Ending LBA for test span 5	Read and Write
82-337	Reserved	Reserved
338-491	Vendor specific	Vendor specific
492-499	Current LBA under test	Read
500-501	Current span under test	Read
502-503	Feature flags R/W	Read and Write
504-507	Vendor Specific	Vendor specific
508-509	Selective self test pending time	Read and Write
510	Reserved	Reserved
511	Data structure checksum	Read and Write

9-6 SMART Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector. LBA Low and Sector Count registers shall be set to specify the log address and sector number to be written.

9-7 SMART Enable Operations (subcommand D8h)

This subcommand enables access to all SMART capabilities. Prior to receipt of a SMART Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of SMART—either enabled or disabled—will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

9-8 SMART Disable Operations (subcommand D9h)

This subcommand disables all SMART capabilities. After receipt of this subcommand the device disables all SMART operations. Non self-preserved Attribute Values will no longer be monitored. The state of SMART—either enabled or disabled—is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute auto saving. After receipt of the SMART Disable Operations subcommand from the host, all other SMART subcommands except SMART Enable Operations are disabled and will be aborted by the device returning the error code as specified in “SMART Error Codes”.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a SMART Read Attribute Values or a SMART Save Attribute Values command.

9-9 SMART Return Status (subcommand DAh)

This subcommand is used to communicate the reliability status of the device to the host's request. Upon receipt of the SMART Return Status subcommand the device saves any updated Attribute Values to the reserved sector, and compares the updated Attribute Values to the Attribute Thresholds.

9-10 SMART Enable/Disable Automatic Off-line (subcommand DBh)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that cause the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities. The Sector Count register shall be set to specify the feature to be enabled or disabled:

Sector Count Feature Description

00h Disable Automatic Off-line
F8h Enable Automatic Off-line

A value of zero written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic off-line data collection feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation such as during a power-on, during a power-off sequence, or during an error recovery sequence. A value of F8h written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic Off-line data collection feature to be enabled. Any other non-zero value written by the host into this register before issuing this subcommand is vendor specific and will not change the current Automatic Off-Line Data Collection and Off-line Read Scanning status. However, the device may respond with the error code specified in “SMART Error Codes”.

10. Security

10-1 Default setting

The Flash SSD is shipped with master password set to 20h value (ASCII blanks) and the lock function disabled. The system manufacturer/dealer may set a new master password by using the SECURITY SET PASSWORD command, without enabling the lock function.

10-2 Initial setting of the user password

When a user password is set, the drive automatically enters lock mode by the next powered-on

10-3 SECURITY mode operation from power-on

In locked mode, the Flash SSD rejects media access commands until a SECURITY UNLOCK command is successfully completed.

10-4 Password lost

If the user password is lost and High level security is set, the drive does not allow the user to access any data. However, the drive can be unlocked using the master password.

If the user password is lost and Maximum security level is set, it is impossible to access data. However, the drive can be unlocked using the ERASE UNIT command with the master password. The drive will erase all user data and unlock the drive.

11. SATA Optional Features

11-1 Power Segment Pin P11

Pin P11 of the power segment of the device connector may be used by the device to provide the host with an activity indication. The activity indication provided by pin P11 is primarily for use in backplane applications.

11-2 Asynchronous Signal Recovery

Phy may support asynchronous signal recovery for those applications where the usage model of device insertion into a receptacle(power applied at time of insertion) does not apply.

When signal is lost, both the host and the device may attempt to recover the signal. A host or device shall determine loss of signal as represented by a transition from PHYRDY to PHYRDYn, which is associated with entry into states LSI: NoCommErr or LS2:NoComm within the Link layer. Note that negation of PHYRDY does not always constitute a loss of signal. Recovery of the signal is associated with exit from state LS2:NoComm.
If the device attempts to recover the signal before the host by issuing a COMINIT, the device shall return its signature following completion of the OOB sequence which included COMINIT. If a host supports synchronous signal recovery, when the host receives an unsolicited COMINIT, the host shall issue a COMRESET to the device. An unsolicited COMINIT is a COMINIT that was not in response to a preceding COMRESET, as defined by the host not being in the HP2:HR_AwaitCOMINIT state when the COMINIT signal is first received.

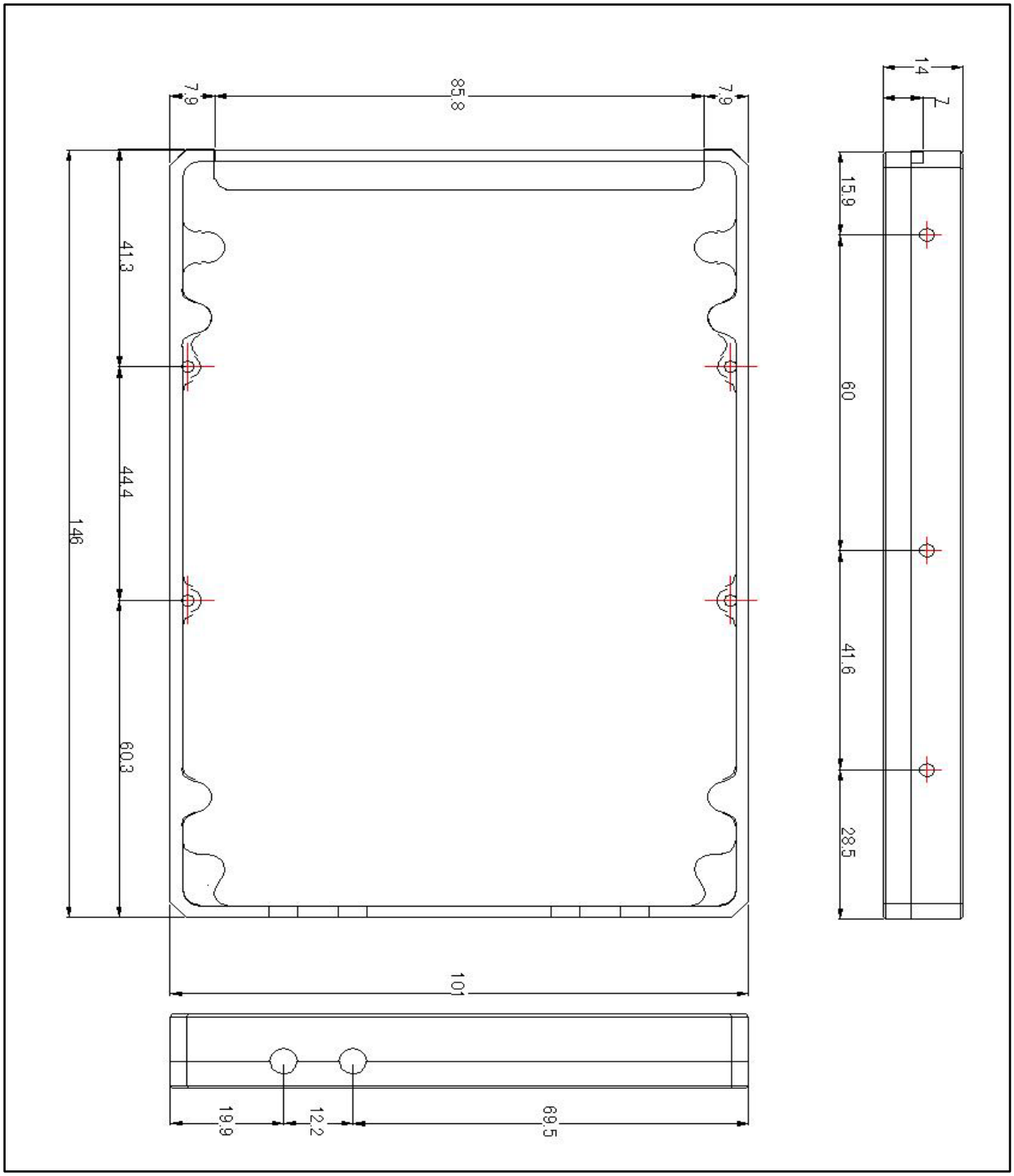
When a COMRESET is sent to the device in response to an unsolicited COMINIT, the host shall set the Status register to 7Fh and shall set all other Shadow Command Block Registers to FFh. When the COMINIT is received in response to the COMRESET which is associated with entry into state HP2B:HR_AwaitNoCOMINIT, the Shadow Status register value shall be updated to either FFh or 80h to reflect that a device is attached.

12. Identify Device Parameters

Word	Contents	Description
0	0C5Ah	General information
1	3FFFh	Number of logical cylinders
2	C837h	Specific configuration
3	0010h	Number of logical heads
4 – 5	0	Retired
6	003Fh	Number of logical sectors per logical track
7 – 8	0	Reserved
9	0000h	Retired
10 -19	XXXX	Serial number(20 ASCII characters)
20	0000h	Retired
21	FFFFh	Buffer Memory Size
22	3000h	Obsolete
23 - 26	XXXX	Firmware revision (8 ASCII characters)
27- 46	XXXX	Model number
47	8001h	Number of sectors on multiple commands
48	0000h	Reserved
49	2F00h	Capabilities
50	4000h	Capabilities
51 - 52	0200h	PIO Mode support
53	0007h	Reserved
54	3FFFh	Number of current logical cylinders
55	0010h	Number of current logical heads
56	003Fh	Number of current logical sectors per track
57	FC10h	Obsolete
58	00FBh	
59	0101h	Multiple sector setting
60	XXXXh	Total number of user addressable sectors (LBA mode only)
61	XXXXh	
62	0000h	Obsolete
63	0007h	Multi-word DMA transfer

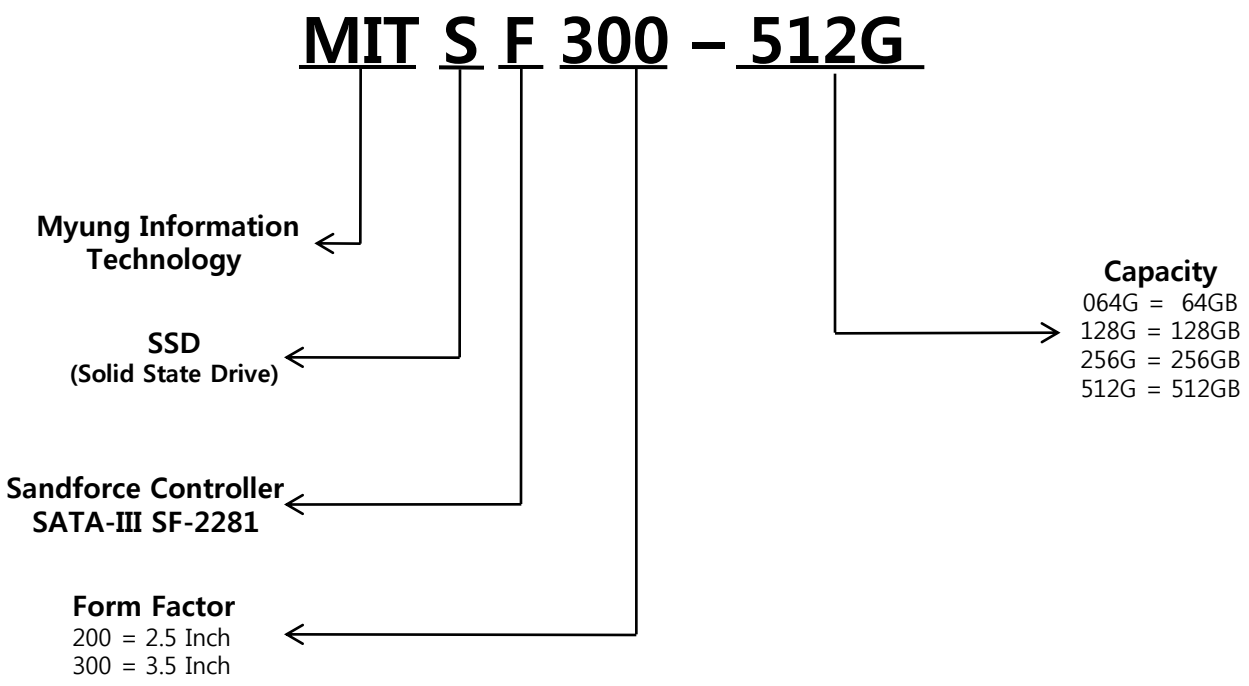
64	0003h	Flow control PIO transfer modes supported
65	0078h	Minimum Multiword DMA transfer cycle time per word
66	0078h	Manufacturer's recommended Multiword DMA transfer cycle time per word
67	0078h	Minimum PIO transfer cycle time without flow control
68	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	4000h	Additional Supported
70 - 74	0	Reserved
75	001Fh	Queue Depth
76	0506h	Serial ATA capability
77	0000h	Reserved
78	0044h	Serial ATA features supported
79	0040h	Serial ATA features enabled
80	01E0h	Major Version Number
81	0000h	Minor Version Number
82	346Bh	Command sets supported
83	7D01h	Command sets supported
84	4022h	Command set/feature supported extension
85	3469h	Command set/feature enabled
86	3C01h	Command set/feature enabled
87	4022h	Command set/feature default
88	407Fh	Ultra DMA transfer
89	0000h	Time required for security erase unit completion
90	0000h	Time required for Enhanced security erase completion
91	0000h	Current advanced power management value
92	0000h	Master Password Revision Code
93	0000h	COMRESET result
94	0000h	Automatic acoustic management value
95	0000h	Stream minimum request size
96 - 99	0	Reserved
100 - 103	XXXX	Maximum user LBA for 48bit address feature set
104-105	0	Reserved

13. Mechanical Specifications



➢Note : All Dimensions are in Millimeters.

14. Ordering Information



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